REMARKS

Claims 1-36 are pending.

The Examiner has objected to the drawings because of a minor error that was introduced when the originally filed drawings were formalized. Applicant is submitting replacement drawings for Figure 5 and Figure 9A that correspond to these drawings as originally filed. Thus, the drawings are not being amended.

The Examiner has objected to the disclosure because the application numbers of cross referenced applications are missing. Applicant has amended the specification to address the Examiner's concern.

The Examiner has rejected claims 1-2, 5-8, 10-21, and 24-36 under 35 U.S.C § 102(b) as being anticipated by Sonnier, claims 3 and 22 under 35 U.S.C § 103(a) as being unpatentable over Sonnier and Jeong, and claim 9 as being unpatentable over Sonnier and Lee. Applicant respectfully disagrees.

Independent claims 1 and 19 recite that the ports of the memory device use a "plesiosynchronous technique" for serial communications. As described in the specification, "the plesiosynchronous clocking technique uses the insertion and removal of symbols by the physical layer of a receiving communication node to compensate for variations in clock frequency between the transmitter and receiver." (Specification, para. 0073.) "A plesiosynchronous clocking technique can be used to avoid the need to transmit a separate clock signal or derive the clock signal from the data signal. (Specification, para. 0010, emphasis added)

The Examiner relies on Sonnier at 68:62-65 as showing a "plesiosynchronous technique." The Examiner states that "T_clock and Rcv clock are of the same frequency." (Office Action, July 23, 2004, pp. 4-5.) Sonnier at 68:45-61, however, makes it clear that a clock signal is transmitted with the data signal. In particular, Sonnier states that "the clock

signal that accompanies the symbol stream, and is used to push symbols onto the clock synchronizing FIFO of the receiving element (router 14, or CPU 12) is substantially identical in frequency." (Sonnier, 68:47-50, emphasis added.)

Since Sonnier teaches that a clock signal accompanies the data signal, Sonnier does not use a "plesiosynchronous technique" in which a separate clock signal is not sent with the data signal. Therefore, Sonnier cannot anticipate the claims.

Based upon the above remarks, applicant respectfully requests reconsideration of this application and its early allowance. If the Examiner has any questions or believes a telephone conference would expedite prosecution of this application, the Examiner is encouraged to call the undersigned at (206) 359-8548.

Dated:

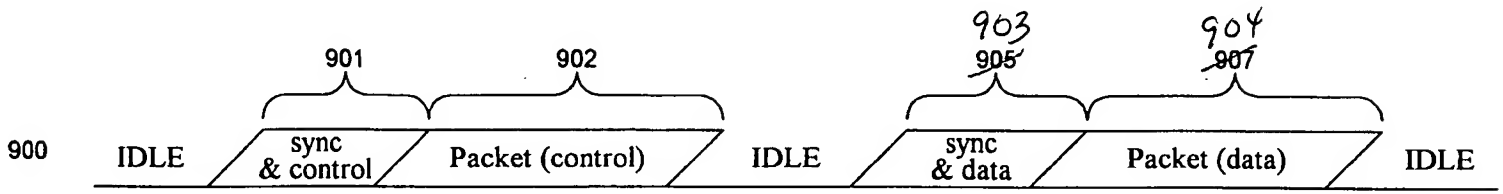
12-21-04

Respectfully submitted,

By Maurice J. Pirio

Maurice J. Pirio
Registration No.: 33,273
PERKINS COIE LLP
P.O. Box 1247
Seattle, Washington 98111-1247
(206) 359-8548
(206) 359-7198 (Fax)
Attorney for Applicant

Attachments



sync & packet type

Fig. 9A

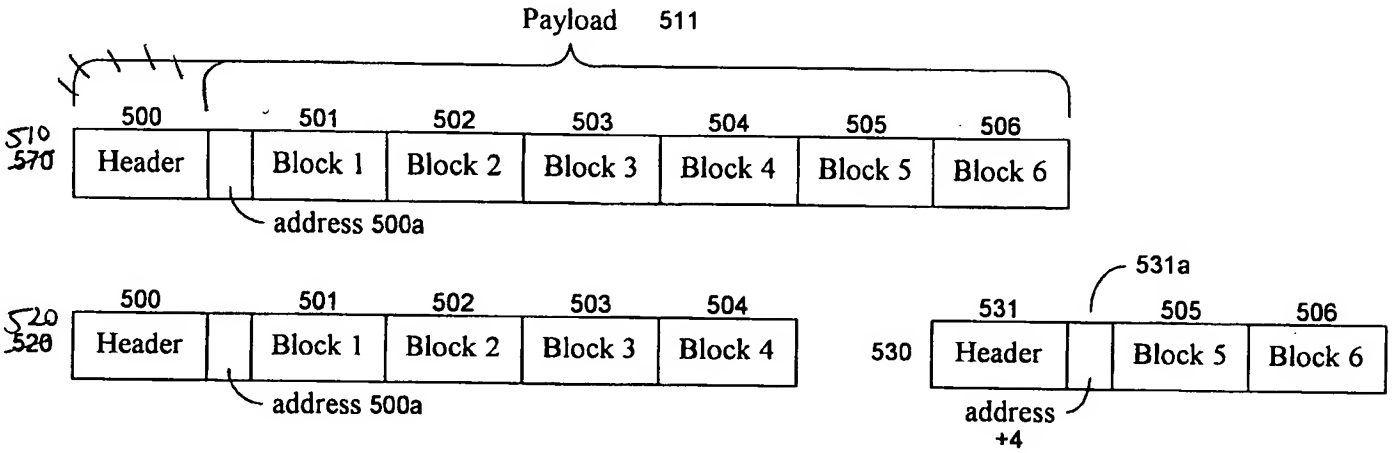


Fig. 5